



### **Replacement Abstract**

A matrix-addressable ferroelectric or electret memory device and a method of operating are explained. The method includes applying a first plurality of voltage difference across a first and a second set of electrodes in the memory when data are read, and applying a second plurality of voltage differences when data are refreshed or rewritten. The first and second plurality of voltage differences correspond to sets of potential levels comprising time sequences of voltage pulses. At least one parameter indicative of a change in a memory cell response is used for determining at least one correction factor for the voltage pulses, whereby the pulse parameter is adjusted accordingly. The memory device comprises means for determining the at least one parameter, a calibration memory connected with means for determining the correction factor, and control circuits for adjusting pulse parameters as applied to read and write operations in the memory device.